IN THE CLAIMS

Please cancel without prejudice claims 1-14.

Please add new claims 15-31 as indicated below.

1. – 14. (Cancelled).

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15. (New)   A memory module controller, comprising:

a first interface circuitry to receive a memory request signal from a system memory

controller over a system memory bus;

a second interface circuitry capable of coupling a plurality of memory devices of a

memory module; and

a control logic coupled to the first interface circuitry and second interface circuitry, in

response to the memory request, to generate a separate signal addressed to and

served by, via the second interface circuitry, at least one of the plurality of

memory devices in a manner specifically required by a specification of the

plurality of memory devices, such that the plurality of memory devices and the

system memory bus operate in different operating environments

16. (New)   The memory module controller of claim 15, further comprising a clock

generator to generate a clock signal to drive the separate signals controlling the plurality

of memory devices, wherein the clock signal is different than a clock signal of the

memory bus.

17. (New)   The memory module controller of claim 16, wherein the first interface circuitry

comprises a request handling logic to examine the memory request to determine whether

the memory request is addressed to at least one of the memory devices and to ignore the memory request if the memory request is not addressed to any of the memory devices.

18. (New)   The memory module controller of claim 17, further comprising a power management unit to control a power supplied to the memory devices.

19. (New)   The memory module controller of claim 18, wherein the plurality of memory devices and the memory bus operate at different power voltages.

20. (New)   The memory module controller of claim 18, wherein the power management unit reduces at least a portion of the power to the memory devices, if the memory request is not addressed to any of the memory devices.

21. (New)   The memory module controller of claim 18, wherein the request handling logic is capable of decoupling the memory devices from the memory bus if the memory request is not addressed to any of the memory devices.

22. (New)   The memory module controller of claim 21, wherein in response to a signal from the request handling logic indicating that the memory request is not addressed to any of the memory devices, the control logic instructs the clock generator to alter a frequency of the clock signal to the memory devices.

23. (New)   The memory module controller of claim 22, wherein the control logic further instructs the power management unit to disable the clock generator if the memory request is not addressed to any of the memory devices, which in turn reduces the power dissipation of the memory devices.

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24. (New)   The memory module controller of claim 15, wherein the memory module is a dual inline memory module (DIMM).

25. (New)   The memory module controller of claim 15, wherein the memory module is a single inline memory module (SIMM).

26. (New)   The memory module controller of claim 15, wherein the plurality of memory devices comprises one of volatile memory devices and non-volatile memory devices.

27. (New)   The memory module controller of claim 15, wherein the first interface circuitry further comprises a handshaking logic to provide a handshake signal to the system memory controller that indicates when the memory module controller is communicating data with the system memory controller.

28. (New)   The memory module controller of claim 15, wherein the first interface circuitry further comprises a data handling logic to receive data from the system memory controller and convert the data into a format specifically required by the specification of the memory devices.

29. (New)   The memory module controller of claim 15, further comprising a writing buffer coupled to the first interface circuitry to store data received from the system memory controller.

30. (New)   The memory module controller of claim 29, further comprising an address storage unit coupled to the write buffer and the first interface circuitry to store addresses associated with the data stored in the write buffer.

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31. (New) The memory module controller of claim 15, further comprising a read buffer coupled to the control logic to store data received from at least one of the plurality of memory devices.